

[METHOD TO RELAX ALIGNMENT ACCURACY REQUIREMENT IN FABRICATION FOR INTEGRATED CIRCUIT]

Abstract

A method to relax the alignment accuracy requirement in an integrate circuit manufacturing is described. The method comprises forming a mask layer over a substrate, and the mask layer comprises a plurality of first openings. Thereafter, a buffer layer fills the first opening, followed by forming a photoresist layer over the substrate. The photoresist layer is then patterned to form a second opening that corresponds to the first opening, and the second opening exposes a portion of the buffer layer. Isotropic etching is then performed to remove the buffer layer exposed by the second opening to expose a sidewall of the first opening that corresponds to the second opening. The photoresist layer is further removed to expose the mask layer that comprises the embedded buffer layer and the opening pattern, which is used as a hard mask layer in a subsequent process.